

1x4 56Gbaud Photodiode Array Chip on Carrier_750um pitch

CPL5012V-1

Features

- InGaAs/InP PIN-PD 1x4 array with integrated back-side lens
- Photodiode pitch 750μm
- Semi-planar structure for high reliability
- Coplanar GSG contact pads

Applications

- 4λ 400GbE TRx

Absolute Maximum Ratings

Parameters	Symbol	Rating	Unit
Reverse voltage	V_R	10	V
Reverse current	I_R	2.5	mA
Forward current	I_F	10	mA
Optical input power	P_{max}	5	dBm
Operating temperature range	T_C	-40 to +85	°C
Storage temperature range	T_{STG}	-40 to +125	°C

Electro-Optical Characteristics

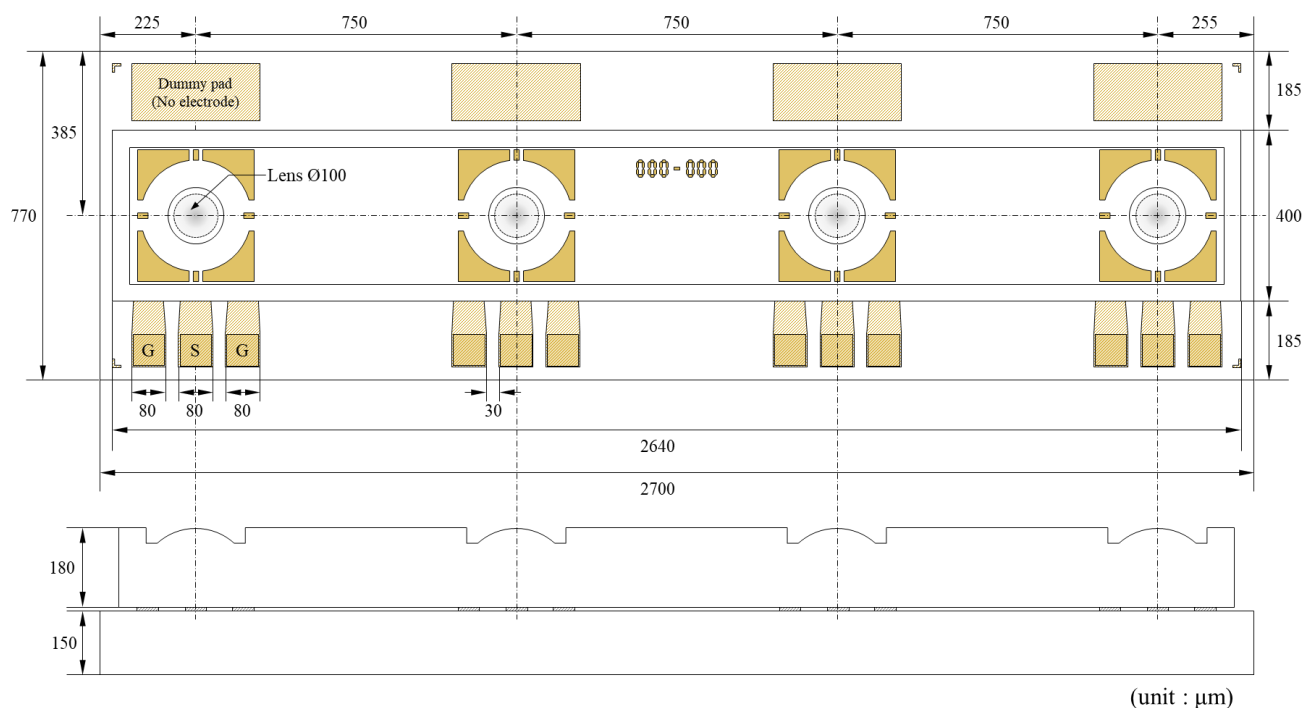
Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating wavelength range	λ	-	1100	-	1640	nm
Responsivity ^{1,2}	R	1310nm, $V_R=2.5V$	-	0.8	-	A/W
Dark current	I_D	$V_R=5.0V$	-	1.0	10	nA
OE Bandwidth	BW	-3dB electrical	-	39	-	GHz
Total capacitance	C	f=1MHz, $V_R=2.5V$	-	0.08	-	pF

1. depend on optical coupling efficiency

2. AR coating is optimized for specific wavelength ($\lambda=1310nm$).

Dimensions

Parameters	Symbol	Size	Unit
PD Chip size	S_c	400 x 2640	μm^2
Carrier size	S_{CoC}	770 x 2700	μm^2
Carrier bonding pad	S_p	80	μm
Diameter of active area	D	12	μm
Photodiode pitch	-	750	μm
Lens ROC	R	110 ± 15	μm
Chip thickness	t	180 ± 15	μm
Carrier thickness	t_c	150 ± 15	μm



Precautio to use

The CPL5012V-1 is sensitive to electrostatic discharge (ESD) and should be handled with appropriate caution. Please use standard ESD protective equipment when handling this product.

Ordering information

CPL5012V-1



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Specifications described here are subject to change without notice